

Introduction

The LatticeMico8™ is an 8-bit microcontroller optimized for Field Programmable Gate Arrays (FPGAs) and Cross-over Programmable Logic Device architectures from Lattice. Combining a full 18-bit wide instruction set with 16 or 32 General Purpose registers, the LatticeMico8 is a flexible Verilog and VHDL reference design suitable for a wide variety of markets, including communications, consumer, computer, medical, industrial, and automotive. The core consumes minimal device resources, less than 200 Look Up Tables (LUTs) in the smallest configuration, while maintaining a broad feature set.

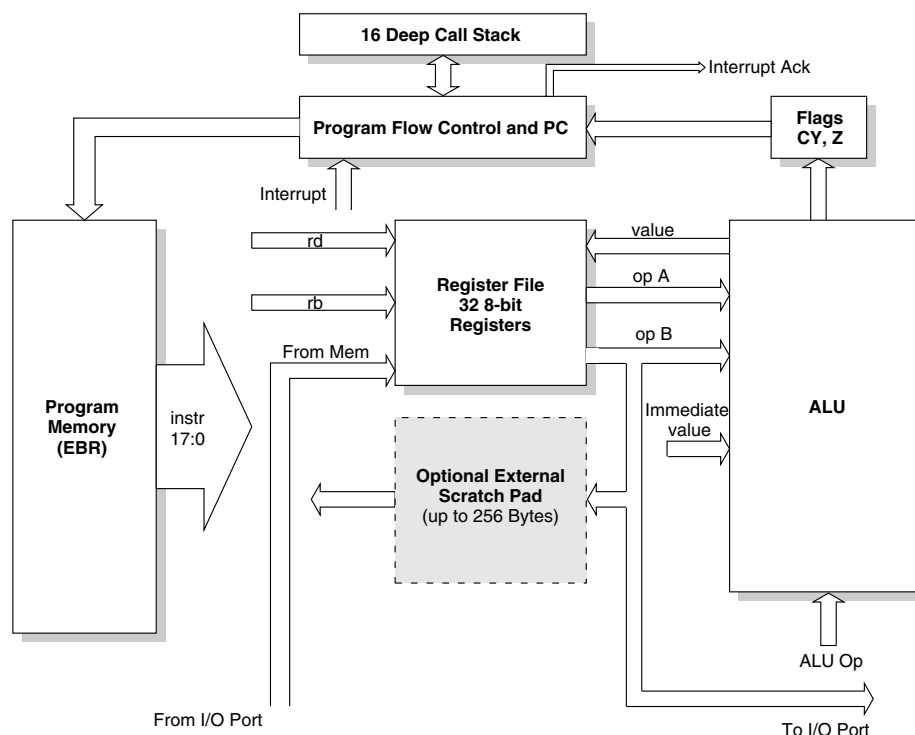
Features

- 8-bit Data Path
- 18-bit Wide Instructions
- Configurable 16 or 32 General Purpose Registers
- Scratch Pad Memory
- Input/Output is Performed Using Paged “Ports” (256 Ports/Page)
- Two/Three Cycles Per Instruction
- Lattice UART Reference Design Peripheral

Functional Description

Figure 1 shows the LatticeMico8 microcontroller block diagram.

Figure 1. LatticeMico8 Microcontroller Block Diagram



Exception Vectors

The LatticeMico8 only provides two exception vectors. One vector address is used when the processor receives a reset, and the other vector is for when the processor receives an interrupt.

Address	Function
0	External Int
1	Reset

Address 0 should contain either a iret or unconditional branch instruction.

General Purpose Registers

The LatticeMico8 processor has either 16 or 32 8-bit general purpose registers. The registers are implemented using a dual port distributed memory. The number of registers is configured prior to synthesizing the processor core.

The LatticeMico8 opcode set always permits the processor to access 32 registers. When the LatticeMico8 is configured with 16 registers any opcode reference to R16 to R31 maps to R0 to R15 respectively.

Page Pointers

Starting with version 3.0 the LatticeMico8 implements page pointers. The page pointers are additional address pins that extend the amount of memory the LatticeMico8 can access.

The LatticeMico8 opcodes can only directly access 256 memory locations. In order to increase the amount of memory the LatticeMico8 can address R15 and R14 have shadow registers. The output from the shadow registers become high-order address bits.

The width of the LatticeMico8 address bus is configurable from eight to 24 bits wide. The address bus presents the concatenation of R15, R14, and 8-bits from the opcode being executed (i.e. $\text{ext_addr} = \text{R15} \ \& \ \text{R14} \ \& \ \text{8-bits opcode}$). The high-order address bits controlled by R15 and R14 become active when the respective register is updated. The low-order 8 bits of the address bus are valid during the second clock of the instruction and remain valid until the cycle terminates.

Scratch Pad RAM

The LatticeMico8 provides an independent memory space that is designed to be used for scratch pad memory.

LatticeMico8, v.2.4 and earlier, implements a 32 byte distributed RAM scratch pad, and allows for up to 256 bytes of external scratch pad memory to be added. When only the internal scratch pad memory is present all 32 bytes of the scratch pad can be accessed using direct and indirect addressing opcodes. When the external scratch pad memory is enabled the internal and external memory spaces become independent areas. The direct memory access opcodes access only the internal scratch pad memory, the indirect addressing opcodes access only the external scratch pad memory. The indirect and direct access types are mutually exclusive when external scratch pad memory is present.

LatticeMico8, v.3.0 and later, changes this model. The scratch pad memory is always external. The scratch pad memory access opcodes always behave orthogonally. Direct addressing always accesses the first 32 bytes of the active scratch pad page. Indirect addressing can access all 256 bytes of the active scratch pad page. V.3.0 scratch pad memory never has an independent internal and external mode, thus the indirect and direct access types are not mutually exclusive.

Hardware (Circular) Call Stack

When a `call` instruction is executed, the address of the next instruction is pushed onto the call stack, a `ret` (return) instruction will pop the stack and continue execution from the location at the top of the stack.

During an interrupt the address of the next instruction is pushed onto the call stack. The processor jumps to the interrupt vector at address 00000. Following an `iret` (return from interrupt) instruction the topmost address in the call stack is popped, and execution resumes from the address retrieved from the stack.

The stack is implemented as a 16 (default) entry circular buffer and any program execution will continue from an undefined location in case of a stack overflow or underflow. A synthesis parameter is available to adjust the size of the call stack.

Interrupt Handling

The microcontroller has one interrupt source, which is level sensitive. The interrupt can be enabled or disabled by software (`cli` = clear interrupt, `sti` = set interrupt). When an interrupt is received, the address of the next instruction is pushed into the call stack and the microcontroller continues execution from the interrupt vector (address 0). The flags (carry and zero) are copied to shadow locations (v.2.4 and earlier), later versions push the flags onto the stack along with the return address. The `interrupt ack` line is set high and the acknowledge line is held high for the entire duration of interrupt handling. Once the interrupt has been acknowledged the interrupt line should be set to 0.

An `iret` instruction will pop the call stack and transfer control to the address on top of the stack. The Flags (carry and zero) are restored from the shadow locations (v.2.4 and earlier), or popped from the call stack (v.3.0 and later). The interrupt acknowledge line is set to low.

The microcontroller cannot handle nested interrupts.

Input/Output

The LatticeMico8 external and scratch pad memory transactions occur synchronously to the LatticeMico8's input clock frequency. The v.2.4 implementation provides an 8-bit address and data bus. The 8-bit address bus permits the LatticeMico8 to access 256 memory locations. The external and scratch pad memories share a single address bus and an output data bus. The input data for each memory is supplied on independent data busses.

The first 32 memory addresses can be accessed using either direct or indirect memory modes. The remaining 224 memory locations can be accessed using only indirect addressing modes.

Figure 2 shows a v.2.4 memory transaction. The address and read/write strobe both appear in the second clock of the processor's decode/execute cycle. The address and strobe only appear for a single clock pulse.

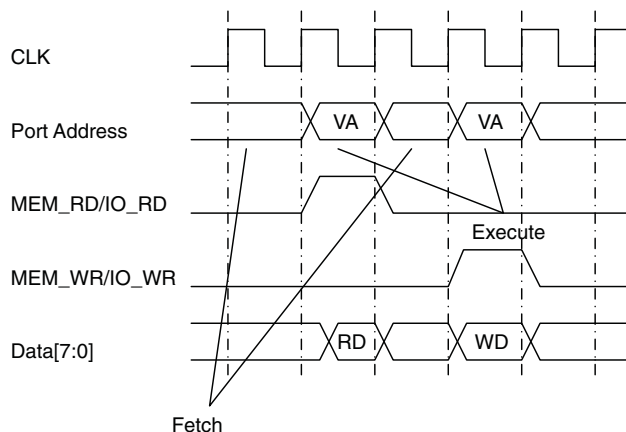
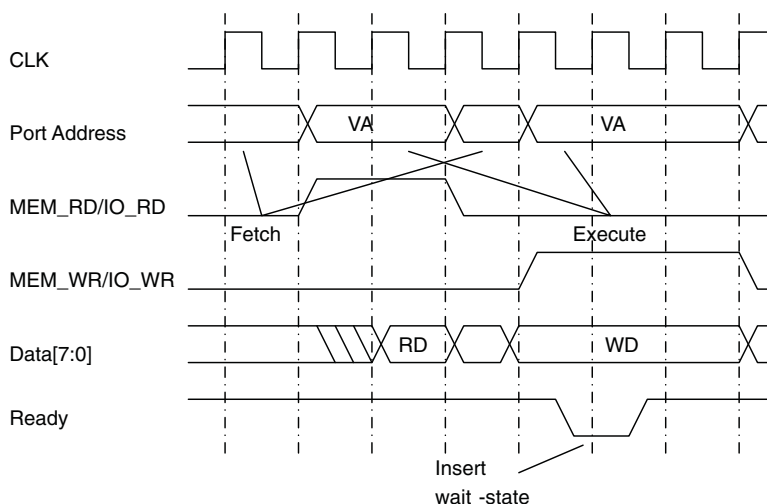
The scratch pad memory read and write strobes, `ext_mem_rd/ext_mem_wr`, go active as the result of the `lsp`, `lspi`, `ssp`, and `sspi` opcodes.

The external port strobes, `ext_io_rd/ext_io_wr`, go active in response to the `import`, `importi`, `export`, `exporti` opcodes.

The v.3.0 (and later) LatticeMico8 implementations modify the memory access times. Both the scratch pad and external memory cycle times are increased by one clock cycle. Figure 3 shows an example of the v.3.0 bus cycle. The v.3.0 bus cycle presents the address for a minimum of two clock cycles. Write data is also presented for a minimum of 2 clock cycles. Read data is captured at the rising clock edge of the third clock cycle.

The v.3.0 core also adds an external ready input. When driven LOW at the beginning of the third clock cycle a wait state is inserted. Wait states continue to be asserted until the `READY` input is driven HIGH coincident to a rising clock edge.

The transition to a three clock cycle memory transaction in v.3.0 permits use of the FPGA's EBR memory. The Lattice EBR requires address be present for one clock prior to the data being read/written. The v.2.4 memory cycle was incompatible with the EBR required behavior.

Figure 2. Version 2.4 Memory Transaction**Figure 3. Version 3.0 Bus Cycle Example**

LatticeMico8 v.3.0 Enhancements

The LatticeMico8 adds some additional capabilities over the earlier versions.

- Addition of a READY signal for memory transactions
- 3 clock cycle memory transactions to support EBR and READY

As described in the previous section the LatticeMico8 memory cycle times have increased by one clock. This gives decode logic time to determine if a memory transaction needs to be lengthened to accommodate slow memory and peripheral devices.

Extended Memory Range Using Page Pointers

A synthesis time enhancement has been made to allow the LatticeMico8 to address more than an 8-bit address space. This is accomplished by adding up to two configurable page pointers. The page pointers are shadow registers that are written whenever R14 and R15 are updated. The shadow registers are combined to make a larger external address bus. The external address is the concatenation of R15, R14, and the address generated as a result of a direct/indirect memory opcode. This permits the LatticeMico8 to address up to 24MB of memory using 65536 256-byte pages.

Increase in Instruction PROM Memory from 512 Lines to User-Defined Depth

The instruction memory size is now configurable using a passed HDL parameter. Sizes from 512 to 4096 lines of code have been tested.

Unconditional Branch/Call Instructions Increased to +/- 2K Instruction Range

The increase in instruction store makes having branch and call instructions with a greater range desirable. Unconditional branch and call opcodes can now be created with a +2047/-2048 range.

Family-Specific Modules Implemented Using PMI

The v.2.4 LatticeMico8 source code was written to support the MachXO™ and LatticeXP™ devices. Migrating between Lattice FPGA families was a bit of effort. V3.0 permits any Lattice FPGA to be a LatticeMico8 host by simply changing the device selected in ispLEVER®.

Flags Pushed Onto the Call Stack

The C and Z flags are pushed onto the stack following any call or interrupt.

LatticeMico8 Synthesis Parameters

The LatticeMico8 core is reconfigurable. There are many parameters available to allow you to tailor the core to your design needs.

Table 1. LatticeMico8 Synthesis Parameters

Parameter Name	Function
FAMILY_NAME	This is a text entry field that is only used during simulation. The value is used to determine the behavioral model to use for instantiated Parameterized Module Instantiation (PMI) elements. Valid entries for this parameter can be found in the ispLEVER Help. This field is not used during synthesis or place and route. The target FPGA device can be changed in ispLEVER, and a new FPGA bitstream image generated without the need to update the FAMILY_NAME entry. ModelSim® can override the value in the HDL using a command line switch when the HDL is compiled.
PROM_FILE	This is a text entry field that determines the opcode data to be loaded into the LatticeMico8 program memory. This parameter can be explicitly entered in the HDL file, or can be updated as a synthesis parameter from Synplify®, Precision RTL®, or ModelSim.
PORT_AW	This defines the number of low order address bits. The value must be less than or equal to 8. The default value is 8, which permits the LatticeMico8 to address up to 256 external ports.
EXT_AW	This defines the size, in bits, of the external address bus. The parameter must be greater than or equal to PORT_AW. The default value is 8, which permits the LatticeMico8 to address 256 ports.
PROM_AW	This defines the number of address bits assigned to the LatticeMico8 program memory. The default value is 9, which permits up to 512 opcodes to be stored.
PROM_AD	This is the number of opcodes the program memory can store and must always be $2^{\text{PROM_AW}}$. The default value is 512 (i.e. 2^9).
REGISTERS_16	This parameter determines how many registers the LatticeMico8 core has. For VHDL the field is a text entry that can be set to TRUE or FALSE. For Verilog the parameter is an integer field that can be either 0 or 1. When the REGISTERS_16 entry is FALSE/0 the LatticeMico8 will have 32 general purpose registers. When it is TRUE/1 it will have 16 general purpose registers.
PGM_STACK_AW	This defines the number of address bits assigned to the LatticeMico8 call stack. The default value is 4, which permits the call stack to hold 16 elements.
PGM_STACK_AD	This defines the depth of the call stack and must always be $2^{\text{PGM_STACK_AW}}$. The default value is 16 (i.e. 2^4).

Instruction Set Description and Encoding

Instruction Set Reference Card:

Operation	Action	Flags
add Rd, Rb	$Rd = Rd + Rb$	CZ
addc Rd, Rb	$Rd = Rd + Rb + \text{Carry}$	CZ
addi Rd, C	$Rd = Rd + \text{Const}$	CZ
addic Rd, Rb	$Rd = Rd + \text{Const} + \text{Carry}$	CZ
and Rd, Rb	$Rd = Rd \& Rb$	Z
andi Rd, C	$Rd = Rd \& \text{Const}$	Z
b label	Branch unconditionally	--
bc label	Branch on carry flag = 1	--
bnc label	Branch on carry flag = 0	--
bnz label	Branch on zero flag = 0	--
bz label	Branch on zero flag = 1	--
call label	Call function	--
callc label	Call function on carry = 1	--
callnc label	Call function on carry = 0	--
callnz label	Call function on zero = 0	--
callz label	Call function on zero = 1	--
clrc	Carry flag = 0	C
clri	Disable interrupts	--
clrz	Zero flag = 0	Z
cmp Rd, Rb	$Rd - Rb$	CZ
cmpi Rd, C	$Rd - \text{Const}$	CZ
export Rd, port#	$(\text{Port}\#) = Rd$	--
exporti Rd, Rb	$(Rb), Rd$	--
import Rd, port#	$Rd = (\text{Port}\#)$	--
importi Rd, Rb	$Rd = (Rb)$	--
iret	Return from interrupt	--
lsp Rd, sp#	$Rd = (\text{sp}\#)$	--
lspi Rd, Rb	$Rd = (Rb)$	--
mov Rd, Rb	$Rd = Rb$	Z
movi Rd, C	$Rd = \text{Const}$	Z
or Rd, Rb	$Rd = Rd \mid Rb$	Z
ori Rd, C	$Rd = Rd \mid \text{Const}$	Z
ret	Return from Call	--
rol Rd, Rb	$Rd = Rb \ll 1, Rb(0) = Rb(7)$	Z
rolc Rd, Rb	$Rd = C:Rb \ll 1, Rb(0) = C$	CZ
ror Rd, Rb	$Rd = Rb \gg 1, Rb(7) = Rb(0)$	Z
rorc Rd, Rb	$Rd = C:Rb \gg 1, C = Rb(0)$	CZ
setc	Carry flag = 1	C
seti	Enable interrupts	--
setz	Zero flag = 1	Z
ssp Rd, sp#	$(\text{sp}\#) = Rd$	--
sspi Rd, Rb	$(Rb) = Rd$	--
sub Rd, Rb	$Rd = Rd - Rb$	CZ
subc Rd, Rb	$Rd = Rd - Rb - \text{Carry}$	CZ
subi Rd, C	$Rd = Rd - \text{Const}$	CZ
subic Rd, C	$Rd = Rd - \text{Const} - \text{Carry}$	CZ
test Rd, Rb	$Rd \& Rb$	Z
testi Rd, C	$Rd \& \text{Const}$	Z
xor Rd, Rb	$Rd = Rd \wedge Rb$	Z
xori Rd, C	$Rd = Rd \wedge \text{Const}$	Z

Please note that for all Branch and Call instructions, the signed offset is represented as binary 2's complement.

ADD RD, Rb

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	Rd	Rd	Rd	Rd	Rd	Rb	Rb	Rb	Rb	Rb	0	0	0

CY Flag Updated	Zero Flag Updated
Yes	Yes

$Rd = Rd + Rb$ (add registers)

The carry flag is updated with the carry out from the addition. The zero flag is set to 1 if all the bits of the result are 0.

ADDI Rd, C

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	1	Rd	Rd	Rd	Rd	Rd	C	C	C	C	C	C	C	C

CY Flag Updated	Zero Flag Updated
Yes	Yes

$Rd = Rd + CCCCCCCC$ (add constant to register)

The carry flag is updated with the carry out from the addition. The zero flag is set to 1 if all the bits of the result are 0.

ADDC Rd, Rb

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	0	Rd	Rd	Rd	Rd	Rd	Rb	Rb	Rb	Rb	Rb	0	0	0

CY Flag Updated	Zero Flag Updated
Yes	Yes

$Rd = Rd + Rb + \text{Carry Flag}$ (add registers and carry flag)

The carry flag is updated with the carry out from the addition. The zero flag is set to 1 if all the bits of the result are 0.

ADDIC Rd, CC

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	1	Rd	Rd	Rd	Rd	Rd	C	C	C	C	C	C	C	C

CY Flag Updated	Zero Flag Updated
Yes	Yes

$Rd = Rd + CCCCCCCC + \text{Carry Flag}$ (add register, constant and carry flag)

The carry flag is updated with the carry out from the addition. The zero flag is set to 1 if all the bits of the result are 0.

SUB Rd, Rb

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	Rd	Rd	Rd	Rd	Rd	Rb	Rb	Rb	Rb	Rb	0	0	0

CY Flag Updated	Zero Flag Updated
Yes	Yes

$Rd = Rd - Rb$ (subtract register from register)

The carry flag is set to 1 if the result is negative. The zero flag is set to 1 if all the bits of the result are 0.

SUBI Rd, C

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	Rd	Rd	Rd	Rd	Rd	C	C	C	C	C	C	C	C

CY Flag Updated	Zero Flag Updated
Yes	Yes

$Rd = Rd - CCCCCCCC$ (subtract constant from register)

The carry flag is set to 1 if the result is negative. The zero flag is set to 1 if all the bits of the result are 0.

SUBC Rd, Rb

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	Rd	Rd	Rd	Rd	Rd	Rb	Rb	Rb	Rb	Rb	0	0	0

CY Flag Updated	Zero Flag Updated
Yes	Yes

$Rd = Rd - Rb - \text{Carry Flag}$ (subtract register with carry from register)

The carry flag is set to 1 if the result is negative. The zero flag is set to 1 if all the bits of the result are 0.

SUBIC Rd, C

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	1	Rd	Rd	Rd	Rd	Rd	C	C	C	C	C	C	C	C

CY Flag Updated	Zero Flag Updated
Yes	Yes

$Rd = Rd - CCCCCCCC - \text{Carry Flag}$ (subtract constant with carry from register)

The carry flag is set to 1 if the result is negative. The zero flag is set to 1 if all the bits of the result are 0.

MOV Rd, Rb

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	0	Rd	Rd	Rd	Rd	Rd	Rb	Rb	Rb	Rb	Rb	0	0	0

CY Flag Updated	Zero Flag Updated
No	Yes

Rd = Rb (move register to register)

The zero flag is set to 1 if all the bits of the result are 0.

MOVI Rd, C

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	1	Rd	Rd	Rd	Rd	Rd	C	C	C	C	C	C	C	C

CY Flag Updated	Zero Flag Updated
No	Yes

Rd = CCCCCCCC (move constant into register)

The zero flag is set to 1 if all the bits of the result are 0.

AND Rd, Rb

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	0	Rd	Rd	Rd	Rd	Rd	Rb	Rb	Rb	Rb	Rb	0	0	0

CY Flag Updated	Zero Flag Updated
No	Yes

Rd = Rd and Rb (bitwise AND registers)

The zero flag is set to 1 if all the bits of the result are 0.

ANDI Rd, C

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	1	Rd	Rd	Rd	Rd	Rd	C	C	C	C	C	C	C	C

CY Flag Updated	Zero Flag Updated
No	Yes

Rd = Rd and CCCCCCCC (bitwise AND register with constant)

The zero flag is set to 1 if all the bits of the result are 0.

OR Rd, Rb

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	0	Rd	Rd	Rd	Rd	Rd	Rb	Rb	Rb	Rb	Rb	0	0	0

CY Flag Updated	Zero Flag Updated
No	Yes

Rd = Rd | Rb (bitwise OR registers)

The zero flag is set to 1 if all the bits of the result are 0.

ORI Rd, C

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	1	Rd	Rd	Rd	Rd	Rd	C	C	C	C	C	C	C	C

CY Flag Updated	Zero Flag Updated
No	Yes

Rd = Rd | CCCCCCCC (bitwise OR register with constant)

The zero flag is set to 1 if all the bits of the result are 0.

XOR Rd, Rb

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	0	Rd	Rd	Rd	Rd	Rd	Rb	Rb	Rb	Rb	Rb	0	0	0

CY Flag Updated	Zero Flag Updated
No	Yes

Rd = Rd and Rb (bitwise XOR registers)

The zero flag is set to 1 if all the bits of the result are 0.

XORI Rd, CC

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	1	Rd	Rd	Rd	Rd	Rd	C	C	C	C	C	C	C	C

CY Flag Updated	Zero Flag Updated
No	Yes

Rd = Rd and CC (bitwise XOR register with constant)

The zero flag is set to 1 if all the bits of the result are 0.

CMP Rd, Rb

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	0	Rd	Rd	Rd	Rd	Rd	Rb	Rb	Rb	Rb	Rb	0	0	0

CY Flag Updated	Zero Flag Updated
Yes	Yes

Subtract Rb from Rd and update the flags. The result of the subtraction is not written back.

The carry flag is set to 1 if the result is negative. The zero flag is set to 1 if all the bits of the result are 0.

CMPI Rd, C

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	1	Rd	Rd	Rd	Rd	Rd	C	C	C	C	C	C	C	C

CY Flag Updated	Zero Flag Updated
Yes	Yes

Subtract Constant from Rd and update the flags. The result of the subtraction is not written back.

The carry flag is set to 1 if the result is negative. The zero flag is set to 1 if all the bits of the result are 0.

TEST Rd, Rb

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	1	0	Rd	Rd	Rd	Rd	Rd	Rb	Rb	Rb	Rb	Rb	0	0	0

CY Flag Updated	Zero Flag Updated
No	Yes

Perform a bitwise AND between Rd and Rb, update the zero flag. The result of the AND operation is not written back.

The zero flag is set to 1 if all the bits of the result are 0.

TESTI Rd, CC

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	1	1	Rd	Rd	Rd	Rd	Rd	C	C	C	C	C	C	C	C

CY Flag Updated	Zero Flag Updated
No	Yes

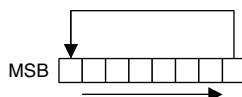
Perform a bitwise AND between Rd and Constant, update the zero flag. The result of the AND operation is not written back.

The zero flag is set to 1 if all the bits of the result are 0.

ROR Rd, Rb

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	0	Rd	Rd	Rd	Rd	Rd	Rb	Rb	Rb	Rb	Rb	0	0	0

CY Flag Updated	Zero Flag Updated
No	Yes

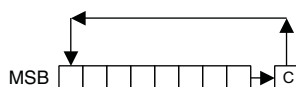


Rotate right. Register B is shifted right one bit, the highest order bit is replaced with the lowest order bit. The result is written back to Register Rd. The zero flag is set to 1 if all the bits of the result are 0.

RORC Rd, Rb

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	0	Rd	Rd	Rd	Rd	Rd	Rb	Rb	Rb	Rb	Rb	0	0	1

CY Flag Updated	Zero Flag Updated
Yes	Yes



Rotate right through carry. The contents of Register B are shifted right one bit, the carry flag is shifted into the highest order bit, the lowest order bit is shifted into the carry flag. The zero flag is set to 1 if all the bits of the result are 0.

ROL Rd, Rb

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	0	Rd	Rd	Rd	Rd	Rd	Rb	Rb	Rb	Rb	Rb	0	1	0

CY Flag Updated	Zero Flag Updated
No	Yes

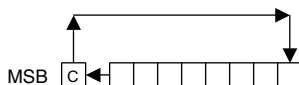


Rotate left. Register B is shifted left by one bit. The highest order bit is shifted into the lowest order bit. The zero flag is set to 1 if all the bits of the result are 0.

ROLC Rd, Rb

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	0	Rd	Rd	Rd	Rd	Rd	Rb	Rb	Rb	Rb	Rb	0	1	1

CY Flag Updated	Zero Flag Updated
Yes	Yes



Rotate left through carry. Register B is shifted left by one bit. The carry flag is shifted into the lowest order bit and the highest order bit is shifted into the carry flag. The zero flag is set to 1 if all the bits of the result are 0.

CLRC

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CY Flag Updated	Zero Flag Updated
Yes	No

Carry Flag = 0

Clear carry flag.

SETC

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1

CY Flag Updated	Zero Flag Updated
Yes	No

Carry Flag = 1

Set carry flag.

CLRZ

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0

CY Flag Updated	Zero Flag Updated
No	Yes

Zero Flag = 0

Clear zero flag.

SETZ

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1

CY Flag Updated	Zero Flag Updated
No	Yes

Zero Flag = 1

Set zero flag.

CLRI

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0

CY Flag Updated	Zero Flag Updated
No	No

Interrupt Enable Flag = 0

Clear interrupt enable flag. Disable interrupts.

SETI

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1

CY Flag Updated	Zero Flag Updated
No	No

Interrupt Enable Flag = 1

Set interrupt enable flag. Enable interrupt.

BZ Label

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	1	0	0	0	L	L	L	L	L	L	L	L	L	L

CY Flag Updated	Zero Flag Updated
No	No

If Zero Flag = 1 then PC = PC + (Signed Offset of Label). Else PC = PC + 1.

Branch if 0. If zero flag is set, the PC is incremented by the signed offset of the label from the current PC. If zero flag is 0, then execution continues with the following instruction. The offset can be +511/-512.

BNZ Label

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	1	0	0	1	L	L	L	L	L	L	L	L	L	L

CY Flag Updated	Zero Flag Updated
No	No

If Zero Flag = 0 then PC = PC + (Signed Offset of Label). Else PC = PC + 1.

Branch if not 0. If zero flag is not set, the PC is incremented by the signed offset of the label from the current PC. If zero flag is set, then execution continues with the following instruction. The offset can be +511/-512.

BC Label

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	1	0	1	0	L	L	L	L	L	L	L	L	L	L

CY Flag Updated	Zero Flag Updated
No	No

If Carry Flag = 1 then PC = PC + (Signed Offset of Label). Else PC = PC + 1.

Branch if carry. If carry flag is set, the PC is incremented by the signed offset of the label from the current PC. If carry flag is not set, then execution continues with the following instruction. The offset can be +511/-512.

BNC Label

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	1	0	1	1	L	L	L	L	L	L	L	L	L	L

CY Flag Updated	Zero Flag Updated
No	No

If Carry Flag = 0 then $PC = PC + (\text{Signed Offset of Label})$. Else $PC = PC + 1$.

Branch if not carry. If carry flag is not set, the PC is incremented by the signed offset of the label from the current PC. If carry flag is set, then execution continues with the following instruction. The offset can be +511/-512.

B Label

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	1	1	L	L	L	L	L	L	L	L	L	L	L	L

CY Flag Updated	Zero Flag Updated
No	No

Unconditional Branch. $PC = PC + \text{Signed Offset of Label}$

Unconditional branch. PC is incremented by the signed offset of the label from the current PC. The offset can be +2047/-2048.

CALLZ Label

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	1	1	0	0	0	L	L	L	L	L	L	L	L	L	L

CY Flag Updated	Zero Flag Updated
No	No

If Zero Flag = 1, then

Push $PC + 1/C/Z$ into Call Stack

$PC = PC + \text{Signed Offset of LABEL}$

Else, $PC = PC + 1$

CALL if 0. If the zero flag is set, the address of the next instruction ($PC+1$) is pushed into the call stack and the PC is incremented by the signed offset (+511/-512) of the label from the current PC. If zero flag is not set, then execution continues from the following instruction.

CALLNZ Label

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	1	1	0	0	1	L	L	L	L	L	L	L	L	L	L

CY Flag Updated	Zero Flag Updated
No	No

If Zero Flag = 0, then

Push $PC + 1/C/Z$ into Call Stack

$PC = PC + \text{Signed Offset of LABEL}$.

Else $PC = PC + 1$

CALL if NOT 0. If the zero flag is not set, the address of the next instruction ($PC+1$) is pushed into the call stack, and the PC is incremented by the signed offset (+511/-512) of the label from the current PC. If the zero flag is set, then execution continues from the following instruction.

CALLC Label

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	1	1	0	1	0	L	L	L	L	L	L	L	L	L	L

CY Flag Updated	Zero Flag Updated
No	No

If Carry Flag = 1, then

Push PC + 1/C/Z into Call Stack

PC = PC + Signed Offset of LABEL.

Else, PC = PC + 1

CALL if carry. If the carry flag is set, the address of the next instruction (PC+1) is pushed into the call stack, and the PC is incremented by the signed offset (+511/-512) of the label from the current PC. If the carry flag is not set, then execution continues from the following instruction.

CALLNC Label

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	1	1	0	1	1	L	L	L	L	L	L	L	L	L	L

CY Flag Updated	Zero Flag Updated
No	No

If Carry Flag = 0, then

Push PC + 1/C/Z into Call Stack

PC = PC + Signed Offset of LABEL

Else, PC = PC + 1

CALL if not carry. If the carry flag is set, the address of the next instruction (PC+1) is pushed into the call stack, and the PC is incremented by the signed offset (+511/-512) of the label from the current PC. If the carry flag is not set, then execution continues from the following instruction.

CALL Label

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	1	1	1	L	L	L	L	L	L	L	L	L	L	L	L

CY Flag Updated	Zero Flag Updated
No	No

Push PC + 1/C/Z into Call Stack

PC = PC + Signed offset of LABEL

Unconditional call. Address of the next instruction (PC+1) is pushed into the call stack, and the PC is incremented by the signed offset (+2047/-2048) of the label from the current PC.

RET

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CY Flag Updated	Zero Flag Updated
Yes	Yes

PC = Top of Call Stack

Pop Call Stack

Restore Zero and Carry Flags from Call Stack

Unconditional return. PC is set to the value on the top of the call stack. The CY and Z flags are restored from the call stack.

IRET

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

CY Flag Updated	Zero Flag Updated
Yes	Yes

PC = Top of Call Stack

Pop Call Stack

Restore Zero and Carry Flags from Call Stack

Return from interrupt. In addition to popping the call stack, the carry and zero flags are restored from shadow locations.

IMPORT Rd, Port#

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	Rd	Rd	Rd	Rd	Rd	P	P	P	P	P	0	0	1

CY Flag Updated	Zero Flag Updated
No	No

Rd = Value from Port (Port#)

Read value from port number (Port#) and write into register Rd. Port # can be 0-31.

IMPORTI Rd, Rb

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	Rd	Rd	Rd	Rd	Rd	Rb	Rb	Rb	Rb	Rb	0	1	1

CY Flag Updated	Zero Flag Updated
No	No

Rd = Value from Port # in Register Rb

Indirect read of port. Value is read from port number in register Rb. Port number can be 0-255.

EXPORT Rd, Port#

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	Rd	Rd	Rd	Rd	Rd	P	P	P	P	P	0	0	0

CY Flag Updated	Zero Flag Updated
No	No

Port Value(Port#) = Rd

Output value of Register D to Port#. Port# can be 0-31.

EXPORTI Rd, Rb

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	Rd	Rd	Rd	Rd	Rd	Rb	Rb	Rb	Rb	Rb	0	1	0

CY Flag Updated	Zero Flag Updated
No	No

Port Value(Rb) = Rd

Output value of Register D to Port# designated by Register B. Port# can be 0-255.

LSP Rd, SS

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	Rd	Rd	Rd	Rd	Rd	S	S	S	S	S	1	0	1

CY Flag Updated	Zero Flag Updated
No	No

Rd = Scratch Pad(SS)

Load from scratch pad memory direct. Load the value from the scratch pad location designated by constant SS into Register D. SS can be 0-31.

LSPI Rd, Rb

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	Rd	Rd	Rd	Rd	Rd	Rb	Rb	Rb	Rb	Rb	1	1	1

CY Flag Updated	Zero Flag Updated
No	No

Rd = Scratch Pad (Rb)

Load from scratch pad memory indirect. Load the value from the scratch pad location designated by Register B into Register D. The location address can be 0-255.

SSP Rd, SS

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	Rd	Rd	Rd	Rd	Rd	S	S	S	S	S	1	0	0

CY Flag Updated	Zero Flag Updated
No	No

Scratch Pad (SS) = Rd

Store into scratch pad memory direct. Store value of register D into scratch pad memory location designated by constant SS. The location address can be 0-31.

SSPI Rd, Rb

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	Rd	Rd	Rd	Rd	Rd	Rb	Rb	Rb	Rb	Rb	1	1	0

CY Flag Updated	Zero Flag Updated
No	No

Scratch Pad (Rb) = Rd

Store into scratch pad memory indirect. Store value of register D, into scratch pad memory location designated by register B. The location address can be 0-255.

Assembler and Instruction Set Simulator

The software tools for the LatticeMico8 microcontroller include an Assembler and an Instruction Set Simulator, both developed in C. The purpose of the Assembler is to generate an Embedded Block RAM (EBR) initialization file from a text assembler input file. The purpose of the Simulator is to execute a program in the host environment. This section describes the use of these tools.

Assembler

The assembler reads in a text assembler source file (default extension .s) and creates one of the following as output:

- Hexadecimal output file (can be used by Module Manager)
- Binary output file (can be used by Module Manager)
- Memory output file (can be used by Module Manager)
- Verilog initialization file (included in design before synthesis)

In addition to these outputs, the Assembler can also generate an assembler listing file.

Command Line

isp8asm -option1 -option2 ... <input filename>

Command Line Options

Option	Comment
-o <filename>	Fully qualified name of the output file.
-s <Program Rom Size>	Default 512 bytes
-l <filename>	Fully qualified name of the listing file.
-vx	Generate output in hexadecimal (default)
-vb	Generate output in binary
-ve	Generate output in Verilog "INIT" format
-vm	Generate output in MEM file format
-?	Help message

Instructions

The Assembler supports all instructions as described in the Instruction Set section.

Pseudo-Ops

The Assembler supports the following pseudo-ops:

<u>Option</u>	<u>Comment</u>
nop	Expanded by the Assembler to mov R0,R0. An instruction without side effects.

Labels

Label definitions are any character sequences ending in a ':'. No other instruction or Assembler directives are allowed in the same line as a label definition.

The Assembler allows both forward and backward references to a label (i.e. it is legal to reference a label before it is defined). Both references in the following example are valid.

```
BackLabel:
    ...
    ...
    b    BackLabel
    ...
    ...
    b    ForwardLabel
    ...
    ...
ForwardLabel:
```

Comments

The character '#' is used as the start of a comment. Everything following the comment character until a new line is ignored by the Assembler.

Constants

The assembler accepts constants in various formats.

- **Hexadecimal values:** Hexadecimal constants must be prefixed with "0x" or "0X". (e.g. 0xFF, 0x12, and 0xAB are all valid hexadecimal constants).
- **Octal values:** Octal values must be prefixed with the numeric character '0'. (e.g. 077, 066, and 012 are valid octal constants).
- **Character constants:** Single character constants must be enclosed in single quotation marks. (e.g. 'A', 'v', '9' are all valid character constants).
- **Decimal constants:** Any sequence of decimal numbers can be a valid constant. (e.g. 123, 255, 231 are valid decimal constants).
- **Location counter:** The special character \$ (dollar sign) is used to give the current value of the location counter.

Note: The hexadecimal, octal, and decimal constants can be optionally prefixed with a '+' or '-' sign.

Assembler Directives

In addition to the instructions described in the Instruction Set section, the Assembler also supports the following directives. An Assembler directive must be prefixed with a '.' character.

- **.org:** This directive allows code to be placed at specific addresses. The syntax for this directive is:
.org <constant>

The constant can be of any form described in the previous section. The Assembler will terminate with an error, if the .org directive is given a location which is less than the current "local counter" value.

- **.equ:** This directive can be used to assign symbolic names to constants. The syntax of the directive is:

```
.equ <symbolic name>,<constant>
.equ newline,'\n'
...
movi r2,newline
```

- **.data:** This directive can be used to embed arbitrary data in the assembler. The syntax for this directive is:

```
.data <constant>
```

The following figure is an example of the listing generated by the Assembler:

Figure 4. Example of Assembler Generated Listing

Loc	Opcode	Opcode		
Counter	(Hex)	(Bin)		
0x0000	0x33001	1100110000000000001	b	start
0x0001		start:		
0x0001	0x10000	0100000000000000000	nop	
0x0002		add:		
0x0002	0x12055	010010000001010101	movi	R00,0x55
0x0003	0x12105	010010000100000101	movi	R01,0x05
0x0004	0x12203	010010001000000011	movi	R02,0x03
0x0005	0x08110	001000000100010000	add	R01,R02
0x0006	0x0A101	001010000100000001	addi	R01,0x01
0x0007	0x10308	010000001100001000	mov	R03,R01
0x0008	0x10410	010000010000010000	mov	R04,R02
0x0009	0x12535	010010010100110101	movi	R05,0x35
0x000A	0x12643	010010011001000011	movi	R06,0x43
0x000B	0x08628	001000011000101000	add	R06,R05
0x000C	0x0A613	001010011000010011	addi	R06,0x13
0x000D	0x10728	010000011100101000	mov	R07,R05
		.		
		.		
		.		

Building Assembler from Source

Although Lattice provides precompiled binary files, the source is available for compilation. The following commands should be used in the Unix and Windows environments.

- **Unix and Cygwin Environments:**

```
gcc -o isp8asm isp8asm.c
```

- **Windows Environment:**

```
cl -o isp8asm_win isp8asm.c
```

Instruction Set Simulator

The software tools for LatticeMico8 include an Instruction Set Simulator for the microcontroller which allows programs developed for the microcontroller to be run and debugged on a host platform. The Simulator can also be used to generate a disassembly listing of a LatticeMico8 program. The Simulator takes as input the memory output file of the Assembler. It emulates the instruction execution of the LatticeMico8 in software. Please note that the Simulator does not handle interrupts.

Command Line

```
<executable filename> -option1 -option2 ... <input filename>
```

Command Line Option

<u>Option</u>	<u>Comment</u>
-p <Program Rom Size>	Default is 512 bytes.
-ix	Program file is in hexadecimal format (default). This is the file generated by the Assembler with the -vx options (default).
-ib	Program file is in binary format. This is the file generated by the Assembler with the -vb option.
-t	Trace the execution of the program. The Simulator will generate a trace as it executes each instruction. It will also print the modified value of any register (if the instruction modifies a register value).
-d	Generate a disassembly of the program specified by the PROM file.

Simulator Interactions

The `import`, `importi` and `export`, `exporti` instructions can be used to interact with the simulator. When an `export`, `exporti` instruction is executed, the simulator will print the value of the port number as well as the contents of the exported register. If the port number is `0xFF`, the simulator will terminate with an exit code identical to the value of the exported register. When an `import`, `importi` instruction is executed, the simulator will issue a prompt containing the port number and read in values from the standard input (`stdin`). The following figure shows an example of a traced simulation. The v.3.0 simulator only implements an 8-bit external address bus.

Figure 5. Example of Trace Simulation

0x00001	0x10000	mov	R00,R00
0x00002	0x12055	movi	R00,0x55
	R00 = 0x55		
0x00003	0x12105	movi	R01,0x05
	R01 = 0x05		
0x00004	0x12203	movi	R02,0x03
	R02 = 0x03		
0x00005	0x08110	add	R01,R02
	R01 = 0x08		
0x00006	0x0A101	addi	R01,0x01
	R01 = 0x09		
0x00007	0x10308	mov	R03,R01
	R03 = 0x09		
0x00008	0x10410	mov	R04,R02
	R04 = 0x03		
0x00009	0x12535	movi	R05,0x35
	R05 = 0x35		
0x0000A	0x12643	movi	R06,0x43
	R06 = 0x43		
0x0000B	0x08628	add	R06,R05
	R06 = 0x78		
0x0000C	0x0A613	addi	R06,0x13
	R06 = 0x8B		
0x0000D	0x10728	mov	R07,R05
	R07 = 0x35		
0x0000E	0x10830	mov	R08,R06
	R08 = 0x8B		
0x0000F	0x12916	movi	R09,0x16
	R09 = 0x16		

```

0x00010      0x12ADF      movi      R10,0xDF
              R10 = 0xDF
              .
              .
              .

```

Building Simulator from Source

Although Lattice provides precompiled binary files, the source is available for compilation. The following commands should be used in the Unix and Windows environments.

- **Unix and Cygwin Environments:**

```
gcc -o isp8sim isp8sim.c
```

- **Windows Environment:**

```
cl -o isp8sim_win isp8sim.c
```

Example

To display the features and capabilities of the LatticeMico8, a demonstration example is also available. It demonstrates the interaction between the timer and the controller and the interrupt capability.

```

# This program will allow user to run a fibonacci number
# generator and updown counter. This program responds to
# the interrupt from the user (through Orcastra).
# When there is an interrupt, the program will halt the current program,
# and execute the int_handler function. When the intr_handler function
# is done, the program will continue from its last position

        b      int_handler
        nop
        nop
        seti                    # set the program to be able to receive interrupt
        nop
        nop
        b start

start:

        import r5, 5

        mov r6, r5
        andi r5, 0xf0           # masking r5 to decide type of program
        mov r7, r5

        mov r5, r6
        andi r5, 0x0f           # masking r5 to get the speed
        mov r25, r5

        cmpi r7, 0x10
        bz phase2
        cmpi r7, 0x20
        bz phase2
        b start

```

phase2:

```

    cmpi r25, 0x01
    bz phase3
    cmpi r25, 0x02
    bz phase3
    cmpi r25, 0x03
    bz phase3
    cmpi r25, 0x04
    bz phase3
    b start

```

phase3:

```

    cmpi r7, 0x10
    bz fibo
    cmpi r7, 0x20          # 1 = fibonacci, 2 = counter
    bz counter
    b start

```

Implementation

Config. Number	Description ¹	Device	LUTs	Registers	SLICES	f _{MAX} (MHz)
1	16 - Regs, 32 byte Ext SP, 512 PROM, 8-bit Ext Address	LFXP3C-4, LFEC3E-4	250	61	144	65.7 (LFXP3C-4) 78.8 (LFEC3E-4)
		LCMX01200C-4	239	61	120	74.0 (LCMX01200C-4)
		LFE2-50E-5	265	61	155	103.5 (LFE2-50E-5)
2	32 - Regs, 32 byte Ext SP, 512 PROM, 8-bit Ext Address	LFXP3C-4, LFEC3E-4	299	61	169	63.9 (LFXP3C-4) 71.7 (LFEC3E-4)
		LCMX01200C-4	290	61	145	77.0 (LCMX01200C-4)
		LFE2-50E-5	308	61	177	98.8 (LFE2-50E-5)
3	16 - Regs, 32 byte Ext SP, 512 PROM, 16-bit Ext Address	LFXP3C-4, LFEC3E-4	255	69	145	66.7 (LFXP3C-4) 76.8 (LFEC3E-4)
		LCMX01200C-4	242	69	121	81.3 (LCMX01200C-4)
		LFE2-50E-5	274	70	157	102.6 (LFE2-50E-5)
4	32 - Regs, 32 byte Ext SP, 512 PROM, 16-bit Ext Address	LFXP3C-4, LFEC3E-4	303	69	168	62.2 (LFXP3C-4) 66.5 (LFEC3E-4)
		LCMX01200C-4	296	69	148	72.5 (LCMX01200C-4)
		LFE2-50E-5	323	69	181	99.2 (LFE2-50E-5)

1. SP = Scratch Pad

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)

e-mail: techsupport@latticesemi.com

Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
—	—	Previous Lattice releases.
March 2007	01.3	Updated B Label, CALL Label, RET and IRET instruction sets.
April 2007	01.4	Corrected IRET instruction.
February 2008	01.5	Added v.3.0 information.